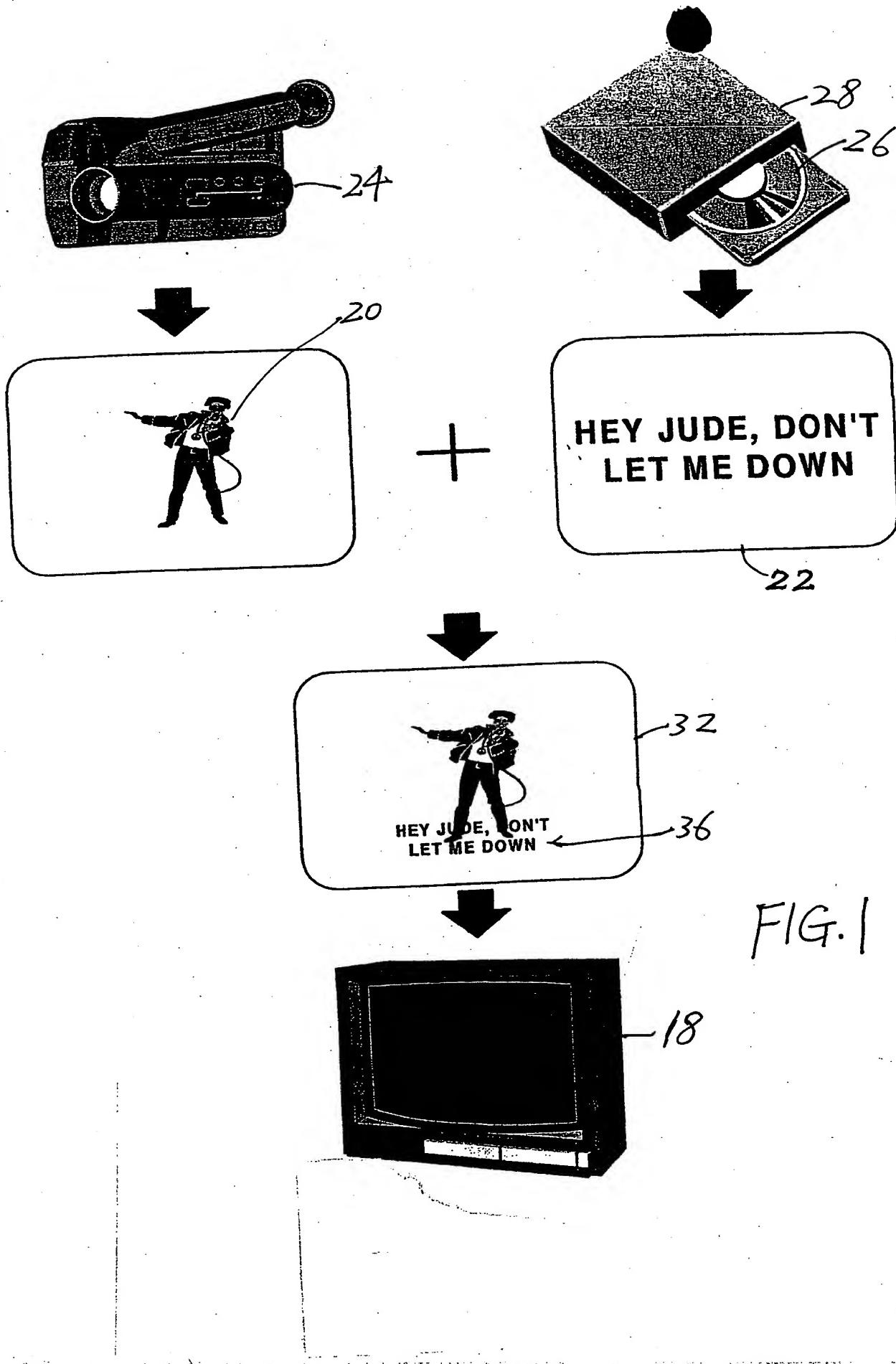


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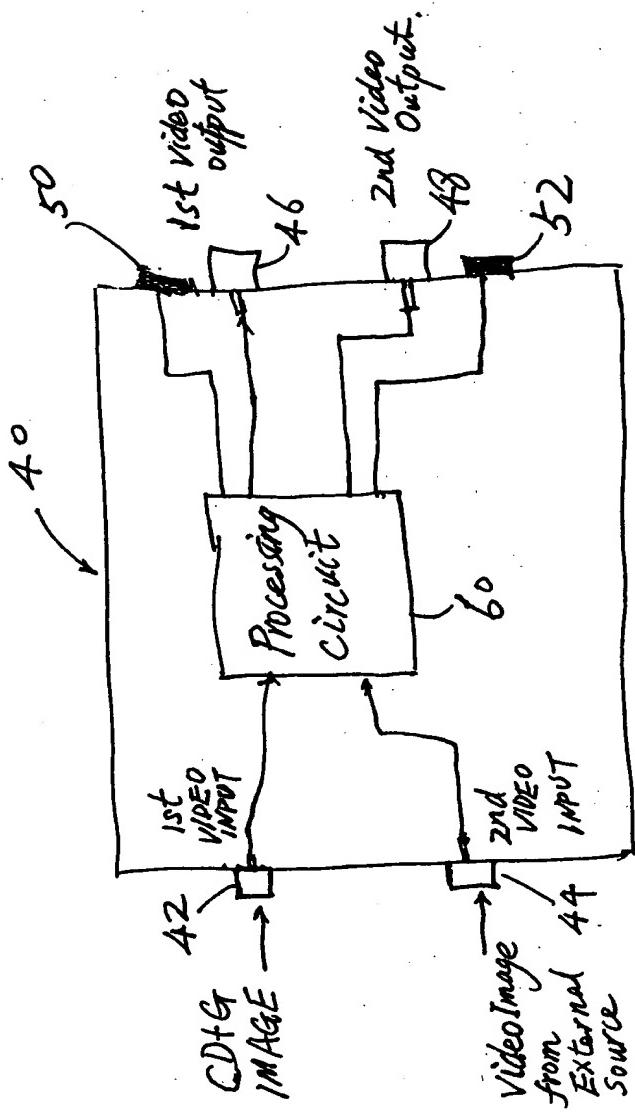


FIG. 2

00000000 00000000 00000000

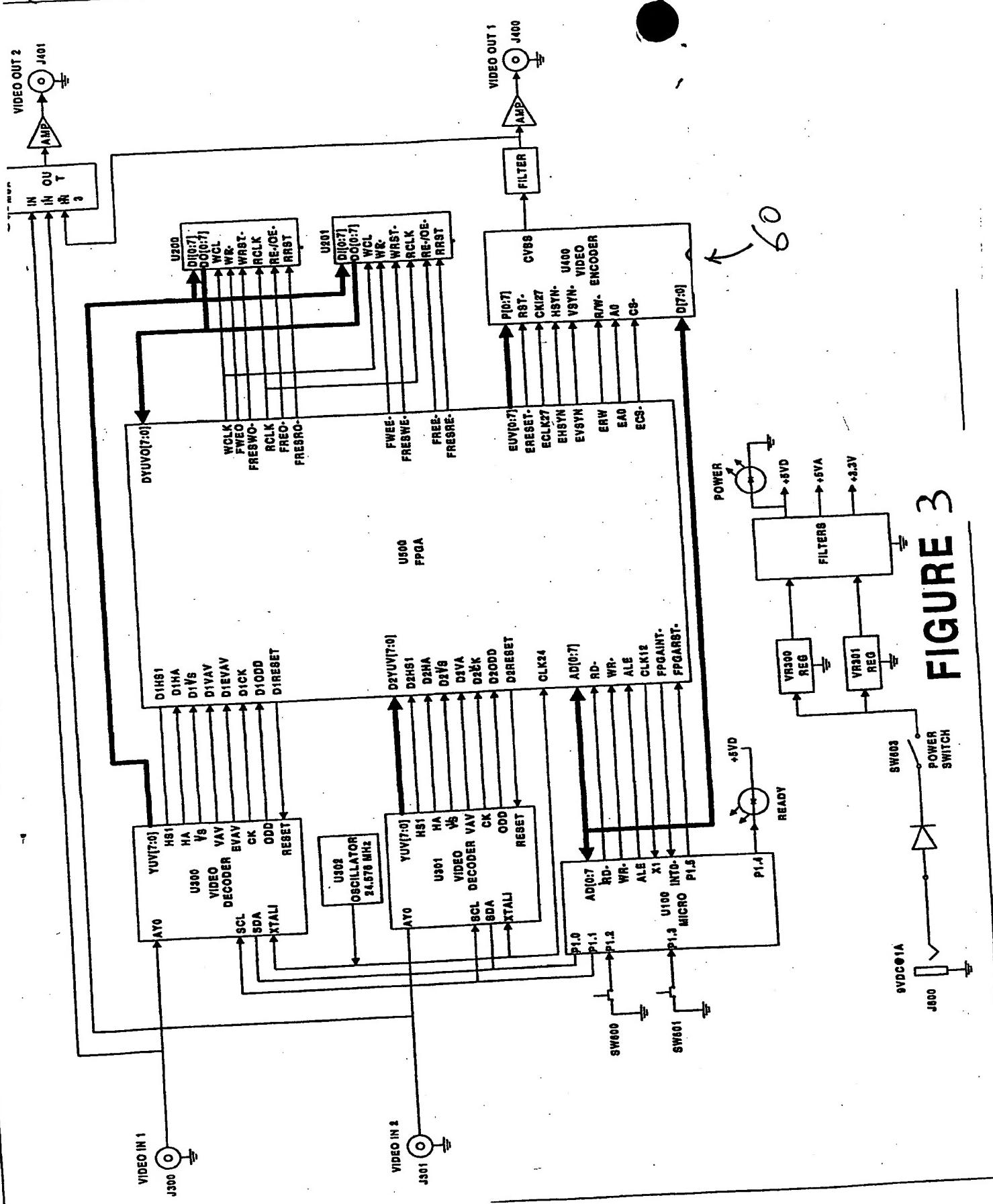
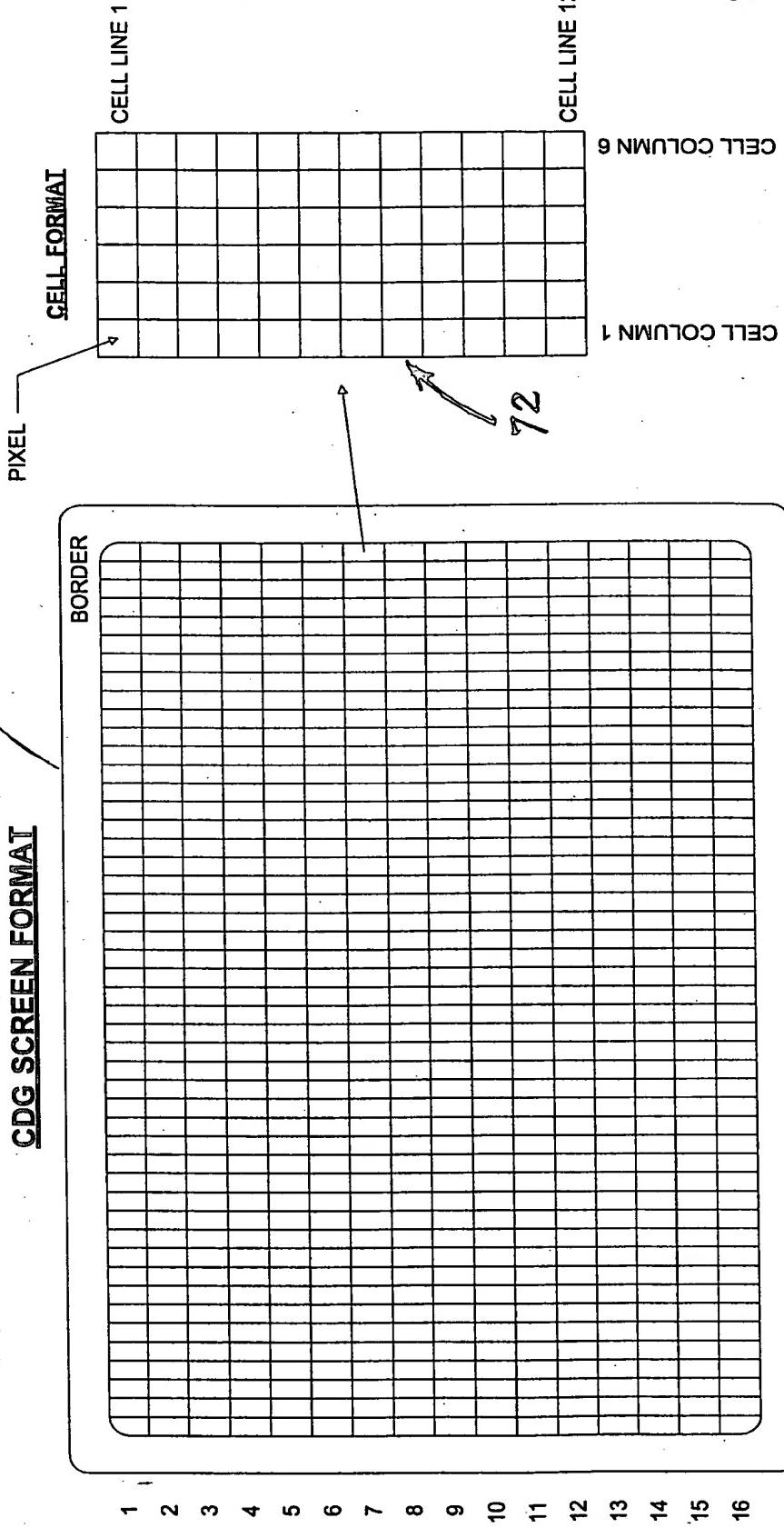


FIGURE 3

70



48

FIG. 4

1

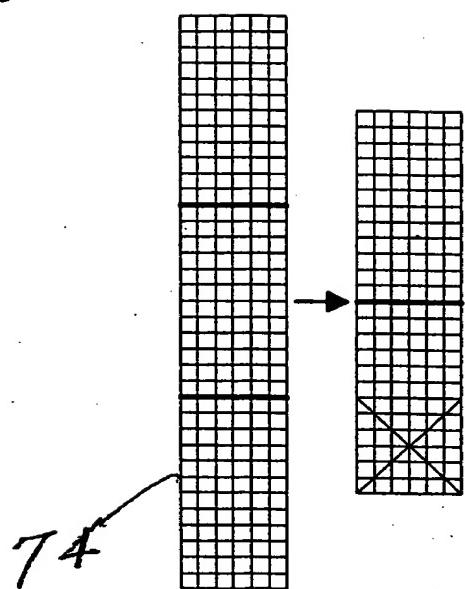


FIG.5

09236906 11212000

CELL START POSITION TRANSLATION	
INPUT CELL LINE	OUTPUT CELL LINE START
1	9
2	9.5
3	10
4	10.5
5	11
6	11.5
7	12
8	12.5
9	13
10	13.5
11	14
12	14.5
13	15
14	15.5
15	16
16	16.5

76

FIG.6

0000000000000000

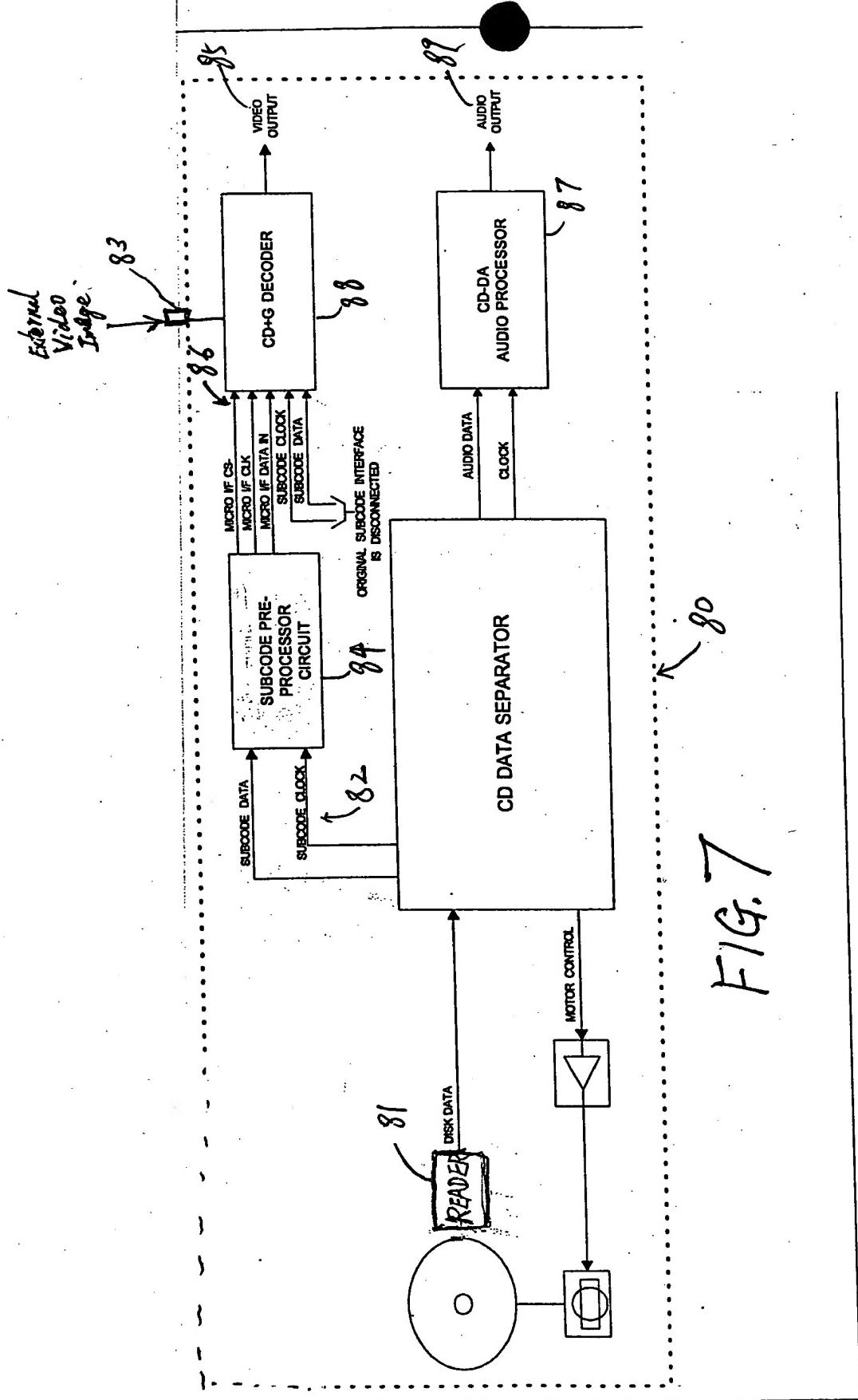
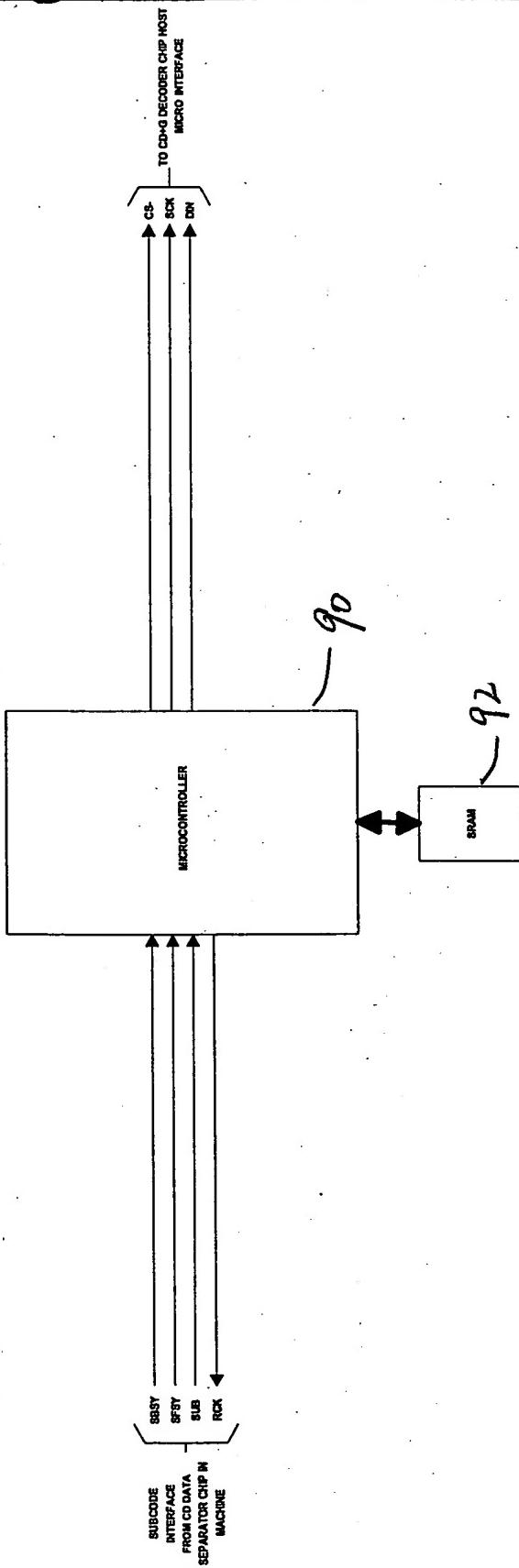


FIG. 7

SUBCODE PRE-PROCESSOR CIRCUIT

✓ 84



F16.8

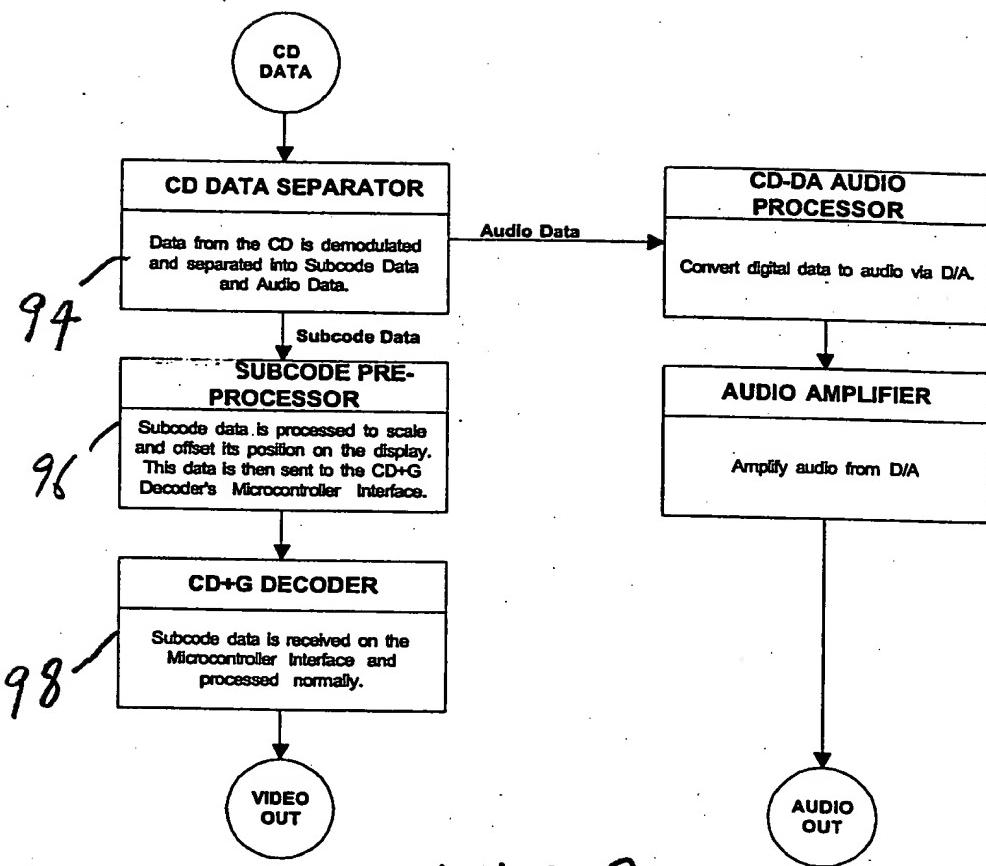


FIG. 9

09246906 - 12/12/2000

00000000000000000000000000000000

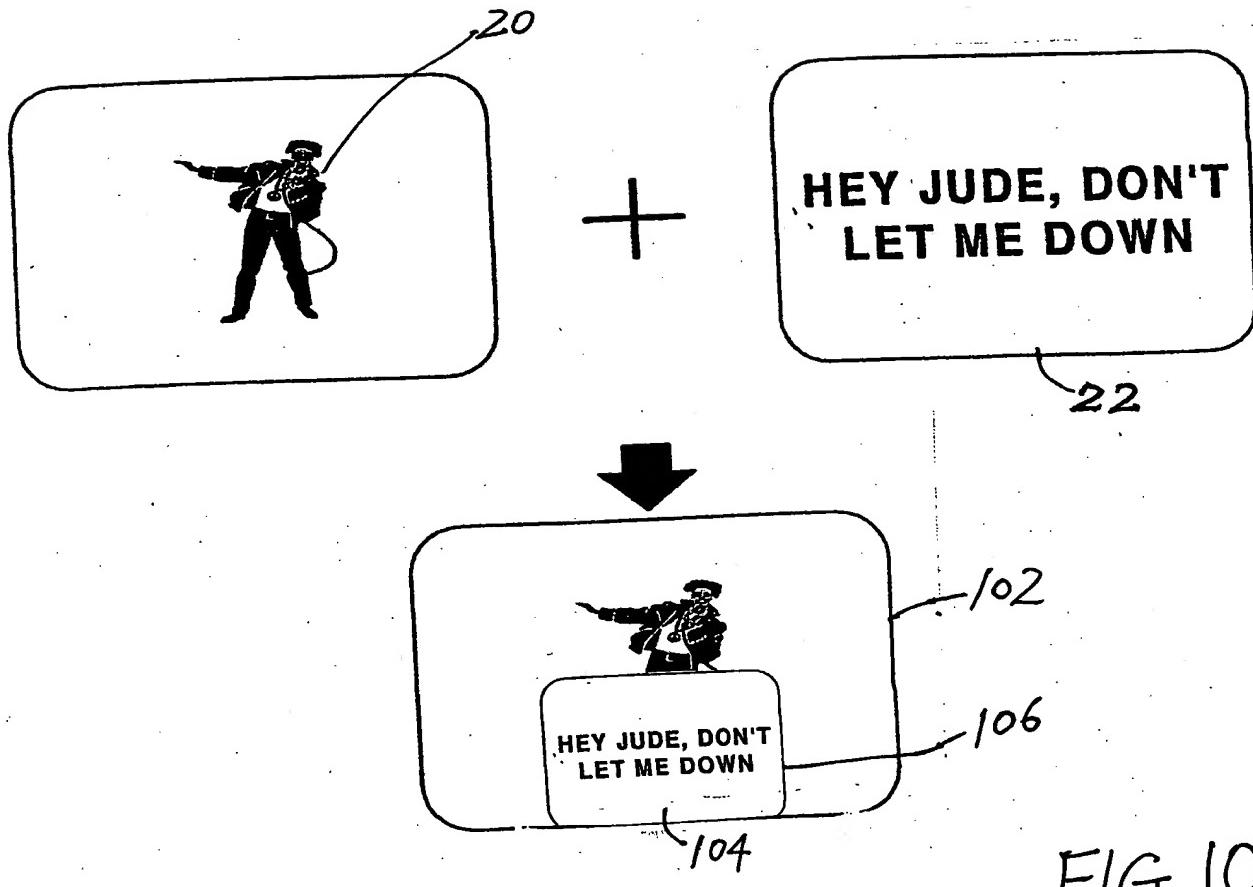


FIG. 10